


Impedance ID	Impedance Signal Layer	Structure Name	Ref. Plane 1 in Layer	Ref. Plane 2 in Layer	Lower Trace Width (W1)	Upper Trace Width (W2)	Trace Separation (S1)	Ground Strip Separation (D1)	Calculated Impedance	Target Impedance	Tol (+/- %)	
9	3	Offset Stripline 1B1A	2	4	3.700	2.700	0.000	0.000	50.130	50.000	10.000	
10	3	Offset Stripline 1B1A	2	4	6.000	5.000	0.000	0.000	40.140	40.000	10.000	
11	3	Edge Coupled Offset Stripline 1B1A	2	4	3.200	2.200	10.000	0.000	99.160	100.000	10.000	
12	3	Edge Coupled Offset Stripline 1B1A	2	4	3.500	2.500	6.250	0.000	89.860	90.000	10.000	
13	6	Coated Microstrip 1B	5	0	8.000	7.000	0.000	0.000	40.160	40.000	10.000	
14	6	Coated Microstrip 1B	5	0	11.100	10.100	0.000	0.000	33.090	33.000	10.000	
15	6	Coated Microstrip 1B	5	0	5.200	4.200	0.000	0.000	50.070	50.000	10.000	
16	6	Edge Coupled Coated Microstrip 1B	5	0	7.800	6.800	4.000	0.000	66.220	66.000	10.000	
17	6	Edge Coupled Coated Microstrip 1B	5	0	4.000	3.000	4.500	0.000	89.900	90.000	10.000	
18	6	Edge Coupled Coated Microstrip 1B	5	0	3.500	2.500	5.800	0.000	99.890	100.000	10.000	
19	6	Edge Coupled Coated Microstrip 1B	5	0	5.400	4.400	4.500	0.000	80.030	80.000	10.000	

Notes

StackName:	Version:	Revision:	Modification:	Date of Revision:	Editor	Pag	
Date: 20-12-2023	Associated Documents:						
Author: -							
Department: Engg-CAM							
Site: www.hiqelectronics.com							